B.Sc. Electronics Syllabus

Semester IV – Paper 4

EL-401T DIGITAL ELECTRONICS AND VERILOG

Unit 1 **12 hours**

Boolean algebra and Logic gates

Boolean algebra- Positive and negative logic. Boolean laws. De Morgan's theorems, simplification of Boolean expressions-SOP and POS. Logic gates- basic logic gates-AND, OR, NOT, logic symbol and truth table. Derived logic gates (NAND,NOR, XOR & XNOR). Universal property of NOR and NAND gates. K-map-3 and 4 variable expressions. Pulse characteristics, logic Families-classification of digital ICs. Characteristics of logic families, circuit description of TTL NAND gate with totem pole and open collector.

TTL IC terminology. Circuit description of CMOS inverter, comparision of TTL and CMOS families.

Unit 2 **12 hours**

Combinational logic circuits

Combinational logic circuits-half adder, full adder, half subtractor, full subtractor. Two bit comparator. Encoder, decimal to BCD priority encoder. 2:4 decoder using AND gates, 3:8 decoder using NAND gates, BCD to decimal decoder, BCD to 7 segment decoder, 4:1 multiplexer, 1:4 demultiplexer using gates. D-A conversion– 4 bit binary weighted resistor type, circuit and working. Circuit of R-2R ladder–concept only.

A-D conversion–characteristics, successive approximation ADC. (mention the relevant ICs for all).

Unit 3 **14 hours**

Sequential logic circuits

RS latch, NAND and NOR latches, Flipflops, clocked RS F/F, edge triggering and level triggering, D F/F and edge triggered J-K F/F, T F/F, edge triggered M/S JK flip flop, clear & preset inputs. Registers and counters- 4bit serial in serial out, serial in Parallel out, parallel in serial out, parallel in parallel out, applications. Ring counter, Johnson counter applications. Asynchronous counters-Logic diagram, Truth table and timing diagrams of 3 bit ripple counter, 3 bit Up-Down counter and modified counters. Synchronous counter- design using K-maps (for mod 3 & mod 5 counters only).

Programmable Logic devices – basic concepts.

Types of PLDs (mention only) - SPLDs–ROM, PLA, PAL and GAL.

CPLD and FPGA.

UNIT 4: **09 hours**

Introduction to Verilog

A Brief History of HDL, Structure of HDL Module, Comparison of VHDL and Verilog Introduction to Simulation and Synthesis Tools, Test Benches.

Verilog: Module, Delays, brief description - data flow style, behavioral style, structural style, mixed design style, simulating design.

Language Elements- Introduction, Keywords, Identifiers, White Space Characters, Comments, format, Integers, reals and strings. Logic Values, Data Types-net types, undeclared nets, scalars and vector nets, Register type, Parameters.

Expressions: Operands, Operators, types of Expressions
Gate level modeling - Introduction, built in Primitive Gates, multiple input gates, Tri-state gates, pull gates, MOS switches, bidirectional switches, gate delay, array instances, implicit nets, Illustrative Examples (both combinational and sequential logic circuits).

UNIT 5: **09 hours**

Data flow Modeling and Behavioral Modeling

Data flow Modeling: Continuous assignment, net declaration assignments, delays, net delays and examples.
Behavioral Modeling: Procedural constructs, timing controls, block statement, procedural assignments, conditional statement, loop statement, procedural continuous assignment, Illustrative Examples

Text books:

1. Digital Fundamentals : Floyd , CBS Publishers
2. Modern Digital Electronics: R.P. Jain, 3rd edition, TMH Publications.
3. A Verilog HDL Primer – J. Bhasker, BSP, 2003 II Edition.
4. Verilog HDL-A guide to digital design and synthesis-SAMIR PALNITKAR, Pearson, 2nd edition.
5. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, 2004 IEEE Press.

Reference books:

1. Digital Principles and applications: Malvino and Leach-TMH 3rd edition
   Digital Systems : Ronald J Tocci, PHI.
2. Design with TTL ICs, Robert L Morries, TMH.
3. Verilog and VHDL by BOTROS.
4. Digital Logic and Compuer design: M. Morris Mano- PHI, new edition
5. Digital Design: M. Morris Mano- PHI 2nd edition, 2000.
6. Digital computer Electronics: Malvino-TMH
7. Digital computer Fundamentals: Thomas C. Bartee-TMH
8. Experiments in digital principles: Malvino and Leach-TMH

Semester IV - Practical IV

EL-401P DIGITAL ELECTRONICS AND VERILOG LAB

Part-A

Experiments in Digital Electronics

1. Characteristics of logic gates 7400, 7402, 7404, 7406,7432
2. Study of logic gates using ICs (7404,7408, 7432,7402,7400,7486,7410) and study of universal property of NAND and NOR gates.
3. Half adder and Full adder using gates.
4. Half subtractor and full subtractor using gates.
5. Clocked RS and D FF using IC 7400 and JK FF using IC 7476.
6. D-A converter-Binary weighted resistor.
7. Shift registers-SISO and SIPO.
8. 4 bit ripple counter using IC 7476 and conversion to decade counter.
9. Decimal to BCD encoder, BCD to 7 segment decoder-7447.
10. Comparator-Study of 4 bit magnitude comparator.
11. Decoder (2:4) using AND gates & (3:8) using 74138
12. Realisation of Full adder and Full subtractor using Mux and Decoder.
13. Study of Multiplexer using IC 74150 and De-Multiplexer using IC 74154.
14. Design and Realization of 4 bit Adder/Subtractor using IC 7483.
15. Design and Realization of BCD Adder using IC 7483.

Note: Minimum of 5 experiments to be performed in part A

Part-B

Experiments in Verilog

1. Write code to realize basic and derived logic gates.
2. Half adder, Full Adder using basic and derived gates.
3. Half subtractor and Full Subtractor using basic and derived gates.
4. Clocked D FF, T FF and JK FF (with Reset inputs).
5. Multiplexer (4x1, 8x1) and Demultiplexer using logic gates.
6. Decoder (2x4, 3x8), Encoders and Priority Encoders.
7. Design and simulation of a 4 bit Adder.
8. Code converters (Binary to Gray and vice versa).
9. 2 bit Magnitude comparator.
10. 3 bit Ripple counter.

Note: Minimum of 5 experiments to be performed in part B